and a gate electrode provided above a channel region between the source/drain regions, said method comprising:

selectively forming a first film on said semiconductor substrate;

etching said semiconductor substrate to form a first groove by using said first film as a mask;

forming a second film in said first groove and thereafter removing said first film;

diffusing an impurity on a surface of said semiconductor substrate to form an impurity diffusion region including a part of a bottom of said first groove by using said second film as a mask;

forming an insulator film on said impurity diffusion region and thereafter removing said second film to form a second groove;

forming a gate insulator film in said second groove so that a top surface of said gate insulator film is higher than a top surface of said impurity diffusion region; and

forming a gate electrode on the top surface of said gate insulator film.

18. (Amended) A method for producing a MIS transistor comprising a semiconductor substrate, source/drain regions formed on the semiconductor substrate, and a gate electrode provided above a channel region between the source/drain regions, said method comprising:

selectively forming a first film on said semiconductor substrate;

etching said semiconductor substrate to form a first groove by using said first film as a mask;

forming a second film in said first groove and thereafter removing said first film;

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diffusing an impurity on a surface of said semiconductor substrate to form an impurity diffusion region including a part of a bottom of said first groove by using said second film as a mask;

forming an insulator film on said impurity diffusion region and thereafter removing said second film to form a second groove;

forming a gate insulator film in said second groove and on said insulator film;

polishing said gate insulator film by using said insulator film as a stopper so that a top surface of said gate insulator film is higher than a top surface of said impurity diffusion region; and

forming a gate electrode on the top surface of said gate insulator film.

22. (Amended) A method for producing a MIS transistor comprising a semiconductor substrate, source/drain regions formed on the substrate, and a gate electrode provided above a channel region between the source/drain regions, said method comprising:

selectively forming a first film on said semiconductor substrate;

diffusing an impurity on a surface of said semiconductor substrate to form an impurity diffusion region including an elevated impurity diffusion region from a channel region by using said first film as a mask;

forming an insulator film on said impurity diffusion region;

removing said first film so as to form a groove;

forming a gate insulator in said groove so that a top surface of said gate insulator film is higher than a top surface of said impurity diffusion region; and

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forming a gate electrode on a top surface of said gate insulator film.

27. (Amended) A method for producing a MIS transistor comprising a semiconductor substrate, source/drain regions formed on the substrate, and a gate electrode provided above a channel region between the source/drain regions, said method comprising:

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selectively forming a first film on said semiconductor substrate;

diffusing an impurity on a surface of said semiconductor substrate to form an impurity diffusion region including an elevated impurity diffusion region from a channel region by using said first film as a mask;

forming an insulator film on said impurity diffusion region;

removing said first film so as to form a groove;

forming a gate insulator in said groove and on said insulator film;

polishing said gate insulator film by using said insulator film as a stopper so that a top surface of said gate insulator film is higher than a top surface of said grooved impurity diffusion region; and

forming a gate electrode on a top surface of said gate insulator film.

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32. (Amended) A method for producing a MIS transistor comprising a semiconductor substrate, source/drain regions formed on the substrate, and a gate electrode provided above a channel region between the source/drain regions, said method comprising:

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forming a dummy film on said channel region, which borders said source drain regions;

selectively depositing semiconductor layers serving as said source/drain regions so that an inclined surface is formed between the top surface of said semiconductor substrate and said channel region;

diffusing an impurity on a surface of said semiconductor substrate to form impurity diffusion regions by using said dummy film as a mask and thereafter removing said dummy film;

depositing an insulator film on an exposed surface of said channel region to form a gate insulator film, which has a cross section of a grooved space at a center thereof; and

depositing a gate electrode on a top of said gate insulator film to form a gate electrode having a cross section of a T shape.

33. (Amended) A method for producing a MIS transistor according to claim 32, further comprising forming a gate insulator film from said insulator film in said second groove so that a top surface of said gate insulator film is higher than a top surface of said grooved impurity diffusion region.

REMARKS

By this Amendment, Applicants propose amending claims 14, 18, 22, 27, 32, and 33 to more clearly recite the features of the present invention, and cancel claims 34-39 without prejudice or disclaimer. Thus, by entry of this Amendment, claims 14-33 are pending.

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